ABSTRACT OF THE DISCLOSURE

Architecture to calibrate read operations in non-volatile memory devices. In one embodiment, a synchronous flash memory is disclosed. The synchronous flash memory includes a read sense amplifier, a verification sense amplifier, a switch, and an output buffer. The switch alternates electrical connection of the output buffer with the read sense amplifier and the verification sense amplifier. By measuring the distributions of voltage thresholds of erased cells versus voltage thresholds of programmed cells, differences in offsets between read state and write state of memory cells are determined. A specific margin is determined to ensure proper reads of the memory cells.

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